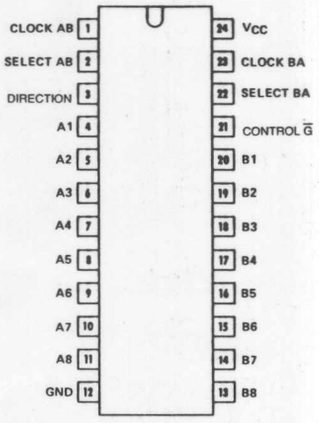
TYPES SN54LS646 THRU SN54LS649
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

D2581, JANUARY 1981

- Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

SN54LS' . . . JT PACKAGE
SN74LS' . . . JT OR NT PACKAGE
(TOP VIEW)

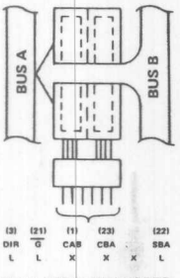


description

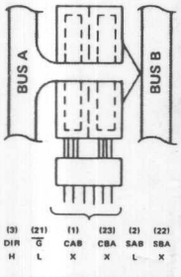
These devices consist of bus transceiver circuits with 3 state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

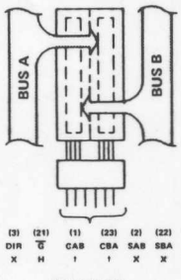
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS646, 'LS647, 'LS648, or 'LS649.



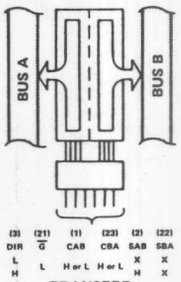
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE



TRANSFER
STORED DATA
TO A OR B

FUNCTION TABLE

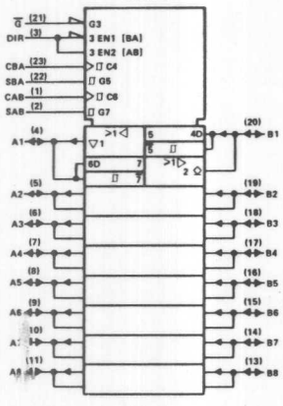
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS646, 'LS647	'LS648, 'LS649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

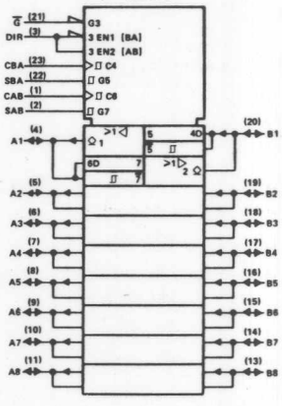
*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

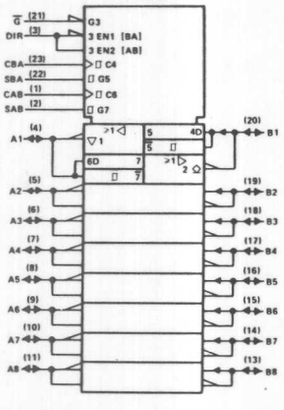
'LS646



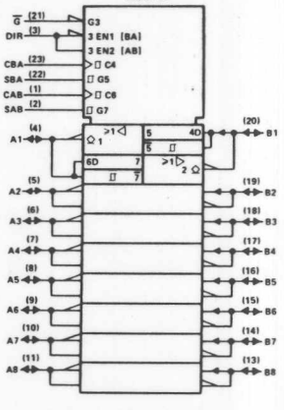
'LS647



'LS648

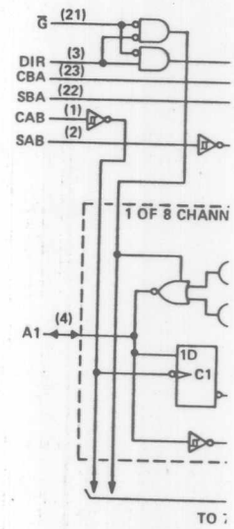


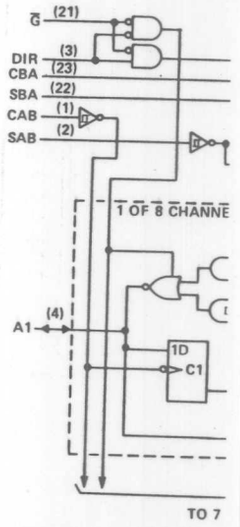
'LS649



TYPES S

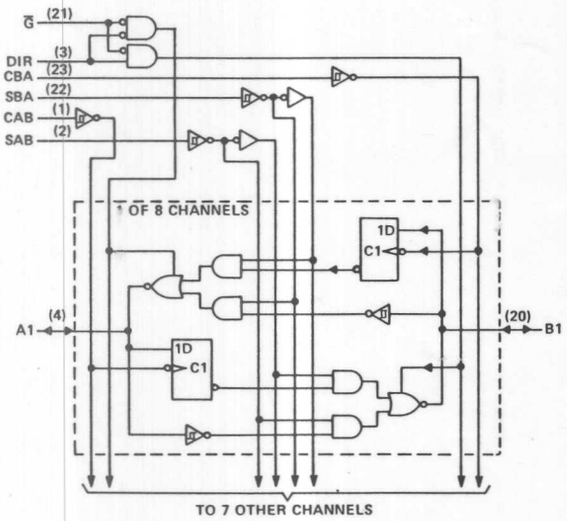
functional block diagram



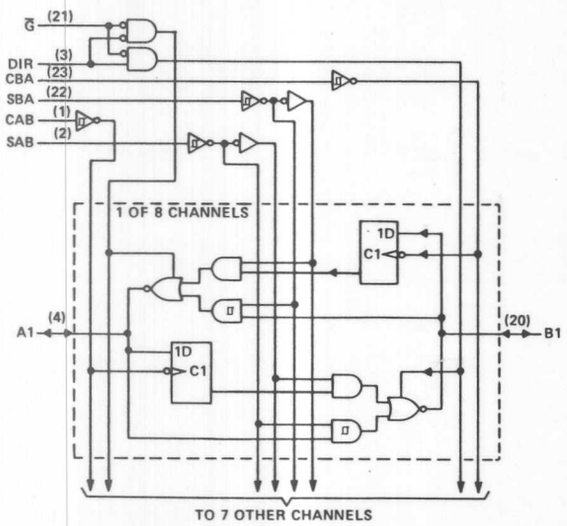


functional block diagram (positive logic)

'LS646, 'LS647

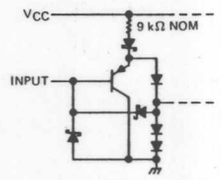


'LS648, 'LS649

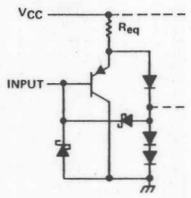


schematics of inputs and outputs

EQUIVALENT OF DIRECTION INPUTS

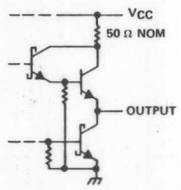


EQUIVALENT OF ALL OTHER INPUTS

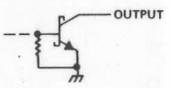


A and B: R_{eq} = 15 kΩ NOM
CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL 'LS646, 'LS648 OUTPUTS



TYPICAL OF ALL 'LS647, 'LS649 OUTPUTS



7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature: SN54LS646, SN54LS648 . . . . . −55°C to 125°C
SN74LS646, SN74LS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−12			−15	mA
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.5			0.6	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{t+} - V_{T-}$), A or B input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_O = 2.7 V			20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX,	V_O = 0.4 V			−400			−400	µA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V		0.1			0.1	mA
		All others		V_I = 7 V		0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶	V_{CC} = MAX,	V_O = 0	−40		−225	−40		−225	mA
I_{CC}	Total supply current	V_{CC} = MAX, Outputs open	Outputs high		91	145		91	145	mA
			Outputs low		103	165		103	165	
			Outputs at Hi-Z		103	165		103	165	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteris

PARAMETER◊	F (I
t_{PLH}	Clo
t_{PHL}	
t_{PLH}	Bus
t_{PHL}	
t_{PLH}	Sele bus high
t_{PHL}	
t_{PLH}	Sele bus low
t_{PHL}	
t_{PZH}	Enal
t_{PZL}	
t_{PZH}	Dire
t_{PZL}	
t_{PHZ}	Enal
t_{PLZ}	
t_{PHZ}	Dire
t_{PLZ}	

t_{PLH} ≡ propagation delay ti
t_{PHL} ≡ propagation delay ti
t_{PZH} ≡ output enable time t
t_{PZL} ≡ output enable time t
t_{PHZ} ≡ output disable time
t_{PLZ} ≡ output disable time t
†These parameters are measu

NOTE 2: Load circuits and v

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		15	25		15	25	ns
t_{PHL}					23	35		24	40	ns
t_{PLH}	Bus	Bus			12	18		12	18	ns
t_{PHL}					13	20		15	25	ns
t_{PLH}	Select, with bus input high†	Bus			33	50		37	55	ns
t_{PHL}					14	25		24	40	ns
t_{PLH}	Select, with bus input low†				26	40		26	40	ns
t_{PHL}					21	35		23	40	ns
t_{PZH}	Enable	Bus			33	55		30	50	ns
t_{PZL}					42	65		37	55	ns
t_{PZH}	Direction				28	45		23	40	ns
t_{PZL}					39	60		30	45	ns
t_{PHZ}	Enable	Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2		23	35		28	45	ns
t_{PLZ}					22	35		22	35	ns
t_{PHZ}	Direction				20	30		24	35	ns
t_{PLZ}					19	30		19	30	ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11

7